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Claims

[c1] 1.A metal-insulator-metal capacitor structure comprising:

a lower conductor layer, wherein said lower conductor layer includes a least one lower capacitor plate and at least one wiring pattern;

at least one capacitor dielectric above said lower capacitor plate;

at least one upper capacitor plate above said capacitor dielectric; and

a hardmask above said upper capacitor plate.

[c2] 2. The structure in claim 1, wherein said hardmask is located along the top and sides of said upper capacitor plate.

[c3] 3.The structure in claim 1, wherein said hardmask has a pattern matching an etched pattern within said lower conductor layer.

[c4] 4.The structure in claim 1, wherein said lower capacitor plate, said capacitor dielectric, and said upper capacitor plate comprise a metal-insulator-metal capacitor.

[c5] 5.The structure in claim 4, wherein said metal-insulator-metal capacitor comprises a single metal-insulator-metal capacitor, wherein said structure further comprises at least one dual metal-insulator-metal capacitor, and wherein said dual metal-insulator-metal capacitor includes a second capacitor dielectric and a second upper plate.

[c6] 6.The structure in claim 1, further comprising an insulator layer covering said hardmask, wherein said hardmask is distinct from said insulator layer.

[c7] 7.The structure in claim 1, wherein spacing between wires in said wiring pattern is approximately one-third the height of said upper capacitor plate above the bottom of said lower capacitor plate.

[c8] 8.A metal-insulator-metal capacitor structure comprising:
a lower conductor layer, wherein said lower conductor layer includes a least one lower capacitor plate and at least one wiring pattern;
at least one capacitor dielectric above said lower capacitor plate;
at least one upper capacitor plate above said capacitor dielectric;
an etch stop layer on said upper capacitor plate; and

a hardmask on said etch stop layer.

[c9] 9. The structure in claim 8, wherein said etch stop layer is located along the top and sides of said upper capacitor plate.

[c10] 10.The structure in claim 8, wherein said hardmask has a pattern matching an etched pattern within said lower conductor layer.

[c11] 11.The structure in claim 8, wherein said lower capacitor plate, said capacitor dielectric, and said upper capacitor plate comprise a metal-insulator-metal capacitor.

[c12] 12.The structure in claim 11, wherein said metal-insulator-metal capacitor comprises a single metal-insulator-metal capacitor, wherein said structure further comprises at least one dual metal-insulator-metal capacitor, and wherein said dual metal-insulator-metal capacitor includes a second capacitor dielectric and a second upper plate.

[c13] 13.The structure in claim 8, further comprising an insulator layer covering said hardmask, wherein said hardmask is distinct from said insulator layer.

[c14] 14.The structure in claim 8, wherein spacing between wires in said wiring pattern is approximately one-third

the height of said upper capacitor plate above the bottom of said lower capacitor plate.

[c15] 15.A method of fabricating a metal-insulator-metal capacitor, said method comprising:
forming a dielectric layer above a lower conductor layer;
patterning an upper conductor layer above said dielectric layer;
forming a hardmask over said upper conductor layer and said dielectric layer;
patterning a photoresist above said hardmask; and
etching said hardmask, said dielectric layer, and said lower conductor layer through said photoresist.

[c16] 16.The method in claim 15, wherein said etching process simultaneously patterns lower capacitor plates and wiring patterns in said lower conductor layer.

[c17] 17.The method in claim 15, wherein said hardmask protects said upper conductor layer from corner rounding during said etching process.

[c18] 18.The method in claim 15, wherein a patterned portion of said upper conductor layer comprises an upper plate of said capacitor, a patterned portion of said lower conductive layer below said upper plate comprises a lower plate of said capacitor, and a patterned portion of said

dielectric layer between said upper plate and said lower plate comprises a capacitor dielectric.

[c19] 19.The method in claim 15, wherein said etching process comprises a multi-step etching process where different etches are used for one or more of said hardmask, said upper conductor layer, said dielectric layer, and said lower conductor.

[c20] 20.The method in claim 15, further comprising, before said process of forming said hardmask:
forming a second dielectric layer above said upper conductor layer; and
patterning a third conductor layer above said upper conductor layer.

[c21] 21.The method in claim 15, wherein said hardmask comprises one of a silicon oxide hardmask and a silicon nitride hardmask.

[c22] 22.A method of fabricating a metal-insulator-metal capacitor, said method comprising:
forming a dielectric layer above a lower conductor layer;
patterning an upper conductor layer above said dielectric layer;
forming an etch stop layer above said upper conductor layer and said dielectric layer;

forming a hardmask over said etch stop layer;
patterning a photoresist above said hardmask; and
etching said hardmask, said etch stop layer, said dielectric layer, and said lower conductor layer through said photoresist.

[c23] 23.The method in claim 22, wherein said etching process simultaneously patterns lower capacitor plates and wiring patterns in said lower conductor layer.

[c24] 24.The method in claim 22, wherein said hardmask protects said upper conductor layer from corner rounding during said etching process.

[c25] 25.The method in claim 22, wherein a patterned portion of said upper conductor layer comprises an upper plate of said capacitor, a patterned portion of said lower conductive layer below said upper plate comprises a lower plate of said capacitor, and a patterned portion of said dielectric layer between said upper plate and said lower plate comprises a capacitor dielectric.

[c26] 26.The method in claim 22, wherein said etching process comprises a multi-step etching process where different etches are used for one or more of said hardmask, said etch stop, said upper conductor layer, said dielectric layer, and said lower conductor.

[c27] 27.The method in claim 22, further comprising, before said process of forming said etch stop layer:
forming a second dielectric layer above said upper conductor layer; and
patterning a third conductor layer above said upper conductor layer.

[c28] 28.The method in claim 22, wherein said hardmask comprises one of a silicon oxide hardmask and a silicon nitride hardmask.